UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/886,741	06/21/2001	Vincent Chan	ATI.0100680	6028

7590 06/27/2005

Christopher J. Reckamp, Esq.
VEDDER, PRICE, KAUFMAN & KAMMHOLZ
222 North LaSalle Street
Chicago, IL 60601

EXAMINER	
CHU, CHRIS C	

ART UNIT	PAPER NUMBER
2815	

DATE MAILED: 06/27/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/886,741	CHAN ET AL.	
	Examiner	Art Unit	
	Chris C. Chu	2815	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *08 June 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *See Continuation Sheet* is/are pending in the application.

4a) Of the above claim(s) *10,14,19,22,26,42,50,52 and 62* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *2 - 9, 11 - 13, 17, 18, 20, 23 - 25, 41, 44 - 48, 53, 54 and 56 - 61* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Continuation of Disposition of Claims: Claims pending in the application are 2 - 14, 17 - 20, 22 - 26, 41, 42, 44 - 48, 50, 52 - 54 and 56 - 62.

DETAILED ACTION

Response to Amendment

1. Applicant's amendment filed on June 8, 2005 has been received and entered in the case.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 2, 5, 6, 8, 9, 12, 13, 41, 44 – 48, 56 and 58 – 61 are rejected under 35 U.S.C. 102(e) as being anticipated by Lu et al. (U. S. Pat. No. 6,294,731).

Regarding claim 56, Lu et al. discloses in e.g., Fig. 1 and Fig. 7 a device comprising:

- a package module (a device in Fig. 7) including a substrate (150) having a standard package footprint;
- an unpackaged semiconductor die (the outermost device of the elements 110; column 7, line 28) directly attached to the package module (see Fig. 7), the unpackaged semiconductor die encapsulated (130 and 140; column 7, line 29) onto the package module in a structure having a planar top surface (see Fig. 7); and

- a packaged semiconductor die (the center device of the elements 110 which is packaged by element 140) having a top surface and attached to the package module;
- wherein the planar top surface of the encapsulated structure and the top surface of the packaged semiconductor die are of equal distance from the substrate (see Fig. 7).

Regarding claim 2, Lu et al. discloses in Fig. 7 the packaged semiconductor being packaged in a ball grid array package (column 7, lines 49 – 51).

Regarding claim 5, Lu et al. discloses a plurality of packaged semiconductors (the center device of the elements 110; column 7, lines 52 – 55) being attached to the package module.

Regarding claim 6, Lu et al. discloses in e.g., Fig. 7 the unpackaged semiconductor die (the outermost device of the elements 110) being wire bonded to the package module (see Fig. 7).

Regarding claim 8, the phrase "wherein attached includes surface-mount technology reflow" is product-by-process limitation. Even though product-by-process claims are limited by and defined by the process, determination of patentability is based upon the product itself. The patentability of a product does not depend on its method of production. If the product in product-by-process claim is the same as or obvious from a product of the prior art, the claim is unpatentable even though the prior product is made by a different process. In re Thorpe, 227 USPQ 964, 966 (Fed. Cir. 1985) (citations omitted). A "product by process" claim is directed to the product per se, no matter how actually made, In re Hirao, **190 USPQ 15 at 17** (footnote 3). See also ln re Brown, **173 USPQ 685**: In re Luck, **177 USPQ 523**; In re Fessmann, **180 USPQ 324**: In re Avery, **186 USPQ 116**; In re Wertheim, **191 USPQ 90 (209 USPQ 254** does not deal with this issue); and ln re Marosi et al., **218 USPQ 289** final product per se which must be

determined in a "product by, all of" claim, and not the patentability of the process, and that an old or obvious product, whether claimed in "product by process" claims or not. Note that Applicant has the burden of proof in such cases, as the above caselaw makes clear.

Regarding claim 9, Lu et al. discloses in e.g., Fig. 7 the encapsulated structure (the element that is encapsulated by the element 130) having a footprint greater than the footprint of the unpackaged semiconductor die (the outermost device of the elements 110).

Regarding claims 12, 48 and 60, since the element (140) of Lu et al. transfers a heat, the element 140 read as a heat sink (column 7, lines 54 – 55). Thus, Lu et al. discloses a planar heat sink adapted to engage the encapsulated structure and the top surface of the packaged semiconductor.

Regarding claim 13, Lu et al. discloses in e.g., Fig. 7 a top surface of the unpackaged semiconductor die and a top surface of the packaged semiconductor being of substantially equal distance from a surface of the package module.

Regarding claim 41, Lu et al. discloses in e.g., Fig. 7 the encapsulated semiconductor die forming a substantially rectangular structure on the package.

Regarding claim 58, Lu et al. discloses in e.g., Fig. 1 and Fig. 7 a multi-die module, comprising:

- a substrate (150) having a first surface and a second surface;
- an unpackaged semiconductor die (the outermost device of the elements 110; column 7, line 28) mounted to the first surface of the substrate, the semiconductor die encapsulated (130 and 140) in a structure having a planar top surface; and

- a packaged semiconductor die (the center device of the elements 110 which is packaged by element 140) having a top surface and mounted on the first surface of the substrate;
- wherein the planar top surface of the encapsulated structure and the top surface of the packaged semiconductor die are of equal distance from the substrate (see Fig. 7).

Regarding claim 44, Lu et al. discloses further including a second packaged semiconductor die (the center device of the elements 110; column 7, lines 52 – 55) mounted on the first surface of the substrate.

Regarding claim 45, Lu et al. discloses in Fig. 7 a plurality of unpackaged semiconductor die mounted on the first surface of the substrate.

Regarding claim 46, Lu et al. discloses in e.g., Fig. 7 the unpackaged semiconductor die being mounted to the first surface of the substrate by wire bonding.

Regarding claim 47, Lu et al. discloses in e.g., Fig. 7 the encapsulating structure (130 and 140) being further comprised of an encapsulating material including epoxy, metal cap (140; column 7, line 55) or silicon coatings.

Regarding claims 59 and 61, Lu et al. discloses in e.g., Fig. 7 a multi-die module, comprising:

- a substrate (150) having a first surface;
- an unpackaged semiconductor die (the outermost device of the elements 110; column 7, line 28) mounted to the first surface of the substrate, the semiconductor die encapsulated (130 and 140) in a structure having a planar top surface; and

- a packaged semiconductor die (the center device of the elements 110 which is packaged by element 140) having a top surface (claim 61) and mounted on the first surface of the substrate, wherein the encapsulating structure is further comprised of an encapsulating material of a metal cap (140); and
- wherein the planar top surface of the encapsulated structure and the top surface of the packaged semiconductor die are of equal distance from the substrate (see Fig. 7).

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 3, 4, 7, 17, 18, 20, 24, 25, 53, 54 and 57 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lu et al. in view of Hannah '232.

Regarding claims 3, 4, 53, 54 and 57, Lu et al. discloses in e.g., Fig. 7 a device comprising:

- a package module (a structure in Fig. 7);
- a die (the outermost device of the elements 110) directly attached to the package module, the die encapsulated (130 and 140) on the package module in a structure having a planar top surface; and

- a packaged die (the center device of the elements 110 which is packaged by element 140) having a top surface and attached to the package module;
- wherein the planar top surface of the encapsulated structure and the top surface of the packaged die are of equal distance from the package module (see Fig. 7).

However, Lu et al. does not disclose the semiconductor dice being graphics-processor die and memory die. However, Hannah teaches in column 3, lines 42 - 46 and column 5, lines 16 - 21 semiconductor dice being a graphics-processor and a memory die. Thus, it would have been obvious to one of ordinary skill in the art at the time when the invention was made to modify Lu et al. by using the semiconductor die to be graphics-processor and memory as taught by Hannah. The ordinary artisan would have been motivated to modify Lu et al. in the manner described above for at least the purpose of receiving commands and graphics data from the main CPU of the computer (column 3, lines 42 - 46).

Regarding claim 7, Lu et al., as modified, discloses the graphics processing die (the outermost device of the elements 110) being wire bonded to the package module (see Fig. 7).

Regarding claim 17, Lu et al., as modified, discloses a plurality of packaged memory (17) being attached to the package module.

Regarding claim 18, Lu et al., as modified, discloses directly attached including the graphics processing die (2) being wire bonded to the package module (see Fig. 7 of Lu et al.).

Regarding claim 20, the phrase "wherein attached includes surface-mount technology reflow" is product-by-process limitation. Even though product-by-process claims are limited by and defined by the process, determination of patentability is based upon the product itself. The patentability of a product does not depend on its method of production. If the product in product-

by-process claim is the same as or obvious from a product of the prior art, the claim is unpatentable even though the prior product is made by a different process. In re Thorpe, 227 USPQ 964, 966 (Fed. Cir. 1985) (citations omitted). A "product by process" claim is directed to the product per se, no matter how actually made, In re Hirao, **190 USPQ 15 at 17** (footnote 3). See also ln re Brown, **173 USPQ 685**: In re Luck, **177 USPQ 523**; In re Fessmann, **180 USPQ 324**: In re Avery, **186 USPQ 116**; In re Wertheim, **191 USPQ 90 (209 USPQ 254** does not deal with this issue); and ln re Marosi et al., **218 USPQ 289** final product per se which must be determined in a "product by, all of" claim, and not the patentability of the process, and that an old or obvious product, whether claimed in "product by process" claims or not. Note that Applicant has the burden of proof in such cases, as the above caselaw makes clear.

Regarding claim 24, since the element (140) of Lu et al. transfers a heat, the element 140 read as a heat sink (column 7, lines 54 – 55). Thus, Lu et al. discloses a heat sink.

Regarding claim 25, Lu et al. discloses in e.g., Fig. 7 a top surface of the graphics-processor die and a top surface of the packaged memory being of substantially equal distance from a surface of the package module (see Fig. 7).

6. Claim 11 is rejected under 35 U.S.C. 103(a) as being unpatentable over Lu et al. in view of Takano et al. '907.

Lu et al. discloses the semiconductor package set forth in the claims except for the standard package sizes being 40mm X 40mm. However, Takano et al. teaches in TABLE 1 a standard package sizes being 40mm X 40mm. Thus, it would have been obvious to one of ordinary skill in the art at the time when the invention was made to modify Lu et al. by using the

standard package sizes as taught by Takano et al. The ordinary artisan would have been motivated to modify Lu et al. in the manner described above for at least the purpose of reducing a limitation in the size of a semiconductor chip (column 2, lines 6 and 7).

7. Claim 23 is rejected under 35 U.S.C. 103(a) as being unpatentable over Lu et al. and Hannah as applied to claim 57 above, and further in view of Takano et al.

Lu et al. and Hannah disclose the semiconductor package set forth in the claims except for the standard package sizes being 40mm X 40mm. However, Takano et al. teaches in TABLE 1 a standard package sizes being 40mm X 40mm. Thus, it would have been obvious to one of ordinary skill in the art at the time when the invention was made to further modify Lu et al. by using the standard package sizes as taught by Takano et al. The ordinary artisan would have been motivated to further modify Lu et al. in the manner described above for at least the purpose of reducing a limitation in the size of a semiconductor chip (column 2, lines 6 and 7).

Response to Arguments

8. Applicant's arguments filed on June 8, 2005 have been fully considered but they are not persuasive.

On page 11, applicant argues that Lu et al. does not show both the planar top surface of the encapsulated structure which encapsulates an unpackaged semiconductor die and a top surface of the package semiconductor die are "of equal" distance from the substrate. This is not persuasive. Lu et al. clearly shows in e.g., Fig. 1 and Fig. 7 the planar top surface of the encapsulated structure (130 and 140; column 7, line 29) which encapsulates an unpackaged

semiconductor die (the outermost device of the elements 110; column 7, line 28) and a top surface of the package semiconductor die (the center device of the elements 110 which is packaged by the element 140) being "of equal" distance from the substrate. In other words, the top surface of the encapsulated structure that contains an unpackaged semiconductor die (the outermost device of the elements 110 which is encapsulated by the elements 130 and 140) is the top surface of the element 140. Also, the top surface of the package semiconductor die (the center device of the elements 110 which is packaged by the element 140) is the top surface of the element 140. Since the top surfaces of both devices have same top surface of the element 140, the top surfaces of both devices are "of equal" distance from the substrate.

For the above reasons, the rejection is maintained.

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Chris C. Chu whose telephone number is 571-272-1724. The examiner can normally be reached on 11:30 - 8:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on 571-272-1664. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Chris C. Chu
Examiner
Art Unit 2815

c.c.
Friday, June 17, 2005

GEORGE ECKERT
PRIMARY EXAMINER